What is claimed is:

1. A sampling frequency conversion apparatus for converting input data of a first sampling frequency into output data of a second sampling frequency, comprising:

storage means into which said input data are continuously written;

interpolation processing means for interpolating the data read out from said storage means to obtain the data of said second sampling frequency;

address difference detector means for detecting an address difference between a write address and a read address in said storage means; and

address control means for optimizing the address difference detected by said address difference detector means; wherein

said address control means adaptively sets a limitation on the optimization operation.

2. A sampling frequency conversion apparatus according to claim 1, wherein

said address control means so works as will not to execute the optimization operation when the address difference detected by said address difference detector means lies within a predetermined range after the passage of a predetermined period of time from the start of supplying the input data.

3. A sampling frequency conversion apparatus according to claim 1, wherein

said address control means so works as will not to execute the optimization operation when the address difference detected by said address difference detector means lies within a predetermined range after the passage of a predetermined period of time from the switching on the power source circuit.

4. A sampling frequency conversion apparatus according to claim 1, wherein

said predetermined period of time is longer than a time required for stabilizing the ratio of the sampling frequency of the input data to the sampling frequency of the output data after the start of supplying said input data.

5. A sampling frequency conversion apparatus according to claim 1, wherein

said address control means so works as will not to execute said optimization operation when the address difference detected by said address difference detector means lies within a predetermined range after the passage of a predetermined period of time from the switching of the input data.

6. A sampling frequency conversion apparatus according to claim 1, wherein

said address control means works to bring said address

difference close to an optimum value imposing no limitation when the predetermined period of time has not been passed after the start of supplying said input data or when the address difference detected by said address difference detector means lies outside the predetermined range.

7. A sampling frequency conversion apparatus according to claim 6, wherein

said address control means executes the control operation for bringing the address difference close to the optimum value by so judging that a moment at which the changing address value exceeds an optimum value or becomes smaller than the optimum value, is the moment of an optimum address difference.

8. A sampling frequency conversion apparatus having a plurality of sampling frequency conversion means for converting a sampling frequency of input data into any sampling frequency to obtain output data, wherein

each of said sampling frequency conversion means includes:

storage means into which said input data are continuously written;

interpolation processing means for interpolating the data read out from said storage means to obtain the data of said second sampling frequency;

address difference detector means for detecting an address difference between a write address and a read address in said storage means; and

address control means for optimizing the address difference detected by said address difference detector means; and wherein,

said address control means so works as will not to execute the optimization operation when the address difference detected by the address difference detector means in each of said sampling frequency conversion means lies within a predetermined range after the passage of a predetermined period of time from the start of supplying said input data, thereby to eliminate a time difference among the output data from said sampling frequency conversion means.

9. A sampling frequency conversion apparatus according to claim 8, wherein

said predetermined period of time is longer than a time required for stabilizing the ratio of the sampling frequency of the input data to the sampling frequency of the output data after the start of supplying the input data.

10. A sampling frequency conversion apparatus according to claim 8, wherein

said address control means works to bring said address difference close to an optimum value when the predetermined period of time has not been passed after the start of supplying said input data or when the address difference detected by said address difference detector means lies outside the predetermined range.

11. A sampling frequency conversion apparatus according

to claim 10, wherein

said address control means executes the control operation for bringing the address difference close to the optimum value by so judging that a moment at which the changing address value exceeds an optimum value or becomes smaller than the optimum value, is the moment of an optimum address difference.